In the Claims:

1. (Currently Amended) A complementary logic circuit, comprising:

a first logic input;

a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a first logic block comprising:

a p-type transistor network ~~of p-type transistors~~ for implementing a predetermined logic function, said network having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal, and said first network gate connection of said p-type transistor network being connected to said first logic input; and

a second logic block comprising:

an n-type transistor network ~~of n-type transistors~~ implementing logic function complementary to said predetermined logic function, said network having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal, and said first network gate

connection of said n-type transistor network being connected to said second logic input;

said inner diffusion connections of said p-type transistor network and of said n-type transistor network being connected to form a common diffusion logic terminal.

2. (Original) A complementary logic circuit according to claim 1, wherein said first and second logic inputs are connected to form a first common logic input.

3. (Original) A complementary logic circuit according to claim 1, wherein each of said logic terminals is separately configurable to serve as a logic input.

4. (Original) A complementary logic circuit according to claim 1, wherein each of said logic terminals is separately configurable to serve as a logic output.

5. (Original) A complementary logic circuit according to claim 1, further comprising a third logic input connected to a second network gate connection of said p-type transistor network.

6. (Original) A complementary logic circuit according to claim 1, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

7. (Original) A complementary logic circuit according to claim 5, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

8. (Original) A complementary logic circuit according to claim 7, said third and fourth logic inputs being connected to form a second common logic input.

9. (Original) A complementary logic circuit according to claim 1, wherein said p-type transistor network comprises a single p-type transistor.

10. (Original) A complementary logic circuit according to claim 1, wherein said n-type transistor network comprises a single n-type transistor.

11. (Currently Amended) A complementary logic circuit according to claim 1, wherein said p-type transistor network ~~of p-type transistors~~ comprises one of a group of networks comprising: a network of p-type field effect transistors (FET), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors.

12. (Currently Amended) A complementary logic circuit according to claim 1, wherein said n-type transistor network ~~of n-type transistors~~ comprises one of a group of networks comprising: a network of n-type FETs, a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors.

13. (Original) A complementary logic circuit according to claim 2, comprising one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate, an inverter gate, and an exclusive OR (XOR) gate.

14. (Original) A complementary logic circuit according to claim 2, wherein said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B.

15. (Original) A complementary logic circuit according to claim 2, wherein said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B.

16. (Original) A logic circuit, comprising interconnected logic elements, said logic elements comprising:

a first logic input;

a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a p-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection; and

an n-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection;

said first logic input being connected to said gate connection of said p-type transistor, said second logic input being connected to said gate connection of said n-type transistor, said first dedicated logic terminal being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal being connected to said outer diffusion connection of said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form a common diffusion logic terminal.

17. (Original) A logic circuit according to claim 16, wherein for each of logic elements said first and second logic inputs are connected to form a common logic input.

18. (Original) A logic circuit according to claim 16, wherein for each of logic elements each of said logic terminals is separately configurable to serve as a logic input.

19. (Original) A logic circuit according to claim 16, wherein for each of logic elements each of said logic terminals is separately configurable to serve as a logic output.

20. (Currently Amended) A logic circuit according to claim 16, wherein a type of said p-type transistors comprises one of a group of transistor types comprising: p-type FET transistors, p-type p-well CMOS transistors, p-type n-well CMOS transistors, p-type twin-well CMOS transistors, p-type SOI transistors, and p-type SOS transistors.

21. (Currently Amended) A logic circuit according to claim 16, wherein said a type of n-type transistors comprises one of a group of transistor types comprising: n-type FET transistors, n-type p-well CMOS transistors, n-type n-well CMOS transistors, n-type twin-well CMOS transistors, n-type SOI transistors, and n-type SOS transistors.

22. (Original) A logic circuit according to claim 17, comprising one of a group of logic circuits comprising: an OR gate, an inverted OR (NOR) gate, an AND gate, a multiplexer gate, an inverter gate, and an exclusive OR (XOR) gate.

23. (Original) A logic circuit according to claim 17, wherein said logic circuit is operable to implement a ((NOT A) OR B) logic operation upon logic inputs A and B.

24. (Original) A logic circuit according to claim 17, wherein said logic circuit is operable to implement a ((NOT A) AND B) logic operation upon logic inputs A and B.

25. (Original) A logic circuit according to claim 16, further comprising at least one stabilizing buffer element.

26. (Original) A logic circuit according to claim 16, further comprising at least one inverter.

27. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a C-element.

28. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a latch.

29. (Original) A logic circuit according to claim 17, comprising one of a group of logic circuits comprising: an SR latch, a D latch, a T latch, and a toggle flip-flop (TFF).

30. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a bundle data filter controller.

31. (Original) A logic circuit according to claim 16, wherein said logic circuit comprises a one to two decoder.

32. (Original) A logic circuit according to claim 16, comprising one of a group of logic circuits comprising: a carry-lookahead adder (CLA), a ripple adder, a combined ripple-CLA adder, a ripple comparator, a multiplier, and a counter.

33. (Currently Amended) A logic circuit, comprising interconnected logic elements, said logic elements comprising:

a first logic input;

a second logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a first logic block comprising:

a p-type transistor network ~~of p-type transistors~~ for implementing a predetermined logic function, said network having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said p-type transistor network being connected to said first dedicated logic terminal, and said first network gate connection of said p-type transistor network being connected to said first logic input; and

a second logic block comprising:

a n-type transistor network ~~of n-type transistors~~ implementing logic function complementary to said predetermined logic function, said network having an outer diffusion connection, a first network gate connection, and an inner diffusion connection,

said outer diffusion connection of said n-type transistor network being connected to said second dedicated logic terminal, and said first network gate connection of said n-type transistor network being connected to said second logic input;

said inner diffusion connections of said p-type transistor network and of said n-type transistor network being connected to form a common diffusion logic terminal.

34. (Original) A logic circuit according to claim 33, wherein for each of said logic elements said first and second logic inputs are connected to form a first common logic input.

35. (Original) A logic circuit according to claim 33, wherein for each of said logic elements each of said logic terminals is separately configurable to serve as a logic input.

36. (Original) A logic circuit according to claim 33, wherein for each of said logic elements each of said logic terminals is separately configurable to serve as a logic output.

37. (Original) A logic circuit according to claim 33, further comprising a third logic input connected to a second network gate connection of said p-type transistor network.

38. (Original) A logic circuit according to claim 33, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

39. (Original) A complementary logic circuit according to claim 37, further comprising a fourth logic input connected to a second network gate connection of said n-type transistor network.

40. (Original) A complementary logic circuit according to claim 39, said third and fourth logic inputs being connected to form a second common logic input.

41. (Original) A logic circuit according to claim 33, wherein said p-type transistor network comprises a single p-type transistor.

42. (Original) A logic circuit according to claim 33, wherein said n-type transistor network comprises a single n-type transistor.

43. (Currently Amended) A logic circuit according to claim 33, wherein said p-type transistor network ~~of p-type transistors~~ comprises one of a group of networks comprising: a network of p-type field effect transistors (FET), a network of p-type p-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type n-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type twin-well complementary metal-oxide semiconductor (CMOS) transistors, a network of p-type silicon on insulator (SOI) transistors, and a network of p-type silicon on sapphire (SOS) transistors.

44. (Currently Amended) A logic circuit according to claim 33, wherein said n-type transistor network ~~of n-type transistors~~ comprises one of a group of networks comprising: a network of n-type FETs, a network of n-type p-well CMOS transistors, a network of n-type n-well CMOS transistors, a network of n-type twin-well CMOS transistors, a network of n-type SOI transistors, and a network of n-type SOS transistors.

45. (Original) A logic circuit according to claim 33, further comprising at least one buffer element.

46. (Original) A logic circuit according to claim 33, further comprising at least one inverter.

47. (Original) A method for designing a logic circuit for performing a given logic function, said logic circuit to be constructed from interconnected logic elements, said logic elements comprising:

a common logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a p-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection; and

an n-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection;

said common logic input being connected to said gate connection of said p-type transistor and to said gate connection of said n-type transistor, said first dedicated logic terminal being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal being connected to said outer diffusion connection of said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form said common diffusion logic terminal, said method comprising the steps of :

setting a synthesized function equal to said given logic function; and

performing a synthesis recursion cycle comprising:

if said synthesized function comprises a single non-inverted logic variable, providing a logic circuit design comprising an input terminal for said non-inverted logic variable and discontinuing said synthesis recursion cycle;

if said synthesized function comprises a high logic signal, providing a logic circuit design comprising a connection to a high logic level, and discontinuing said synthesis recursion cycle;

if said synthesized function comprises a low logic signal, providing a logic circuit design comprising a connection to a low logic level, and discontinuing said synthesis recursion cycle; and

if said synthesized function comprises either an inverted single variable or a multi-variable function, performing the steps of:

extracting a first logic function, and a second logic function from a Shannon expansion of said synthesized function for a selected logic variable;

setting said synthesized function to said first logic function;

performing a synthesis recursion cycle to obtain a circuit design for a first sub-circuit;

setting said synthesized function to said second logic function;

performing a synthesis recursion cycle to obtain a circuit design for a second sub-circuit;

providing a logic circuit design comprising a logic element having an input terminal for said selected logic variable at a common terminal of a logic element, an output of said first sub-circuit connected to the first dedicated logic terminal of said logic element, an output of said second sub-circuit connected to the second dedicated logic terminal of said logic element, and a circuit output at the common diffusion logic terminal of said logic element; and

discontinuing said synthesis recursion cycle.

48. (Original) A method for designing a logic circuit according to claim 47, wherein extracting a first logic function, and a second logic function from a Shannon expansion of said synthesized function for a selected logic variable comprises:

extracting said first logic function from said synthesized function by setting said selected variable to a logic high in said synthesized function; and

extracting said second logic function from said synthesized function by setting said selected variable to a logic low in said synthesized function.

49. (Original) A method for designing a logic circuit according to claim 47, further comprising adding a buffer to said circuit design to provide stabilization for a logic signal.

50. (Original) A method for designing a logic circuit according to claim 47, further comprising adding an inverter to said circuit design to provide stabilization for a logic signal.

51. (Original) A method for providing a logic circuit, from logic elements interconnected so as to implement a required logic function, said logic elements comprising:

a common logic input;

a first dedicated logic terminal;

a second dedicated logic terminal;

a p-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection; and

an n-type transistor, having an outer diffusion connection, a gate connection, and an inner diffusion connection;

said common logic input being connected to said gate connection of said p-type transistor and to said gate connection of said n-type transistor, said first dedicated logic terminal being connected to said outer diffusion connection of said p-type transistor, said second dedicated logic terminal being connected to said outer diffusion connection of

said n-type transistor, and said inner diffusion connection of said p-type transistor and said inner diffusion connection of said n-type transistor being connected to form a common diffusion logic terminal, said method comprising the steps of:

obtaining a logic circuit design by performing the following steps:

setting a synthesized function equal to said required logic function;

performing a synthesis recursion cycle comprising:

if said synthesized function comprises a single non-inverted logic variable, providing a logic circuit design comprising an input terminal for said non-inverted logic variable and discontinuing said synthesis recursion cycle;

if said synthesized function comprises a high logic signal, providing a logic circuit design comprising a connection to a high logic level, and discontinuing said synthesis recursion cycle;

if said synthesized function comprises a low logic signal, providing a logic circuit design comprising a connection to a low logic level, and discontinuing said synthesis recursion cycle; and

if said synthesized function comprises either an inverted single variable or a multi-variable function, performing the steps of:

extracting a first logic function, and a second logic function from a Shannon expansion of said synthesized function for a selected logic variable;

setting said synthesized function to said first logic function;

performing a synthesis recursion cycle to obtain a circuit design for a first sub-circuit;

setting said synthesized function to said second logic function;

performing a synthesis recursion cycle to obtain a circuit design for a second sub-circuit;

providing a logic circuit design comprising a logic element having an input terminal for said selected logic variable at a common terminal of a logic element, an output of said first sub-circuit connected to the first dedicated logic terminal of said logic element, an output of said second sub-circuit connected to the second dedicated logic terminal of said logic element, and a circuit output at the common diffusion logic terminal of said logic element; and

discontinuing said synthesis recursion cycle;

and

connecting said logic elements in accordance with said circuit design.

52. (Original) A method for providing a logic circuit according to claim 51, wherein said extracting said first logic function and said second logic function comprises:

extracting said first logic function from said synthesized function by setting said selected variable to a logic high in said synthesized function; and

extracting said second logic function from said synthesized function by setting said selected variable to a logic low in said synthesized function.

53. (Original) A method for providing a logic circuit according to claim 51, further comprising connecting a buffer between two of said logic elements.

54. (Original) A method for providing a logic circuit according to claim 51, further comprising connecting an inverter between two of said logic elements.